

Summary Descriptions of Projects, 2010-2011

Class-E PA with Envelope Elimination and Restoration via Current-mode DAC

David Allstot (University of Washington)

Abstract - In mobile high-speed communications systems the power amplifier (PA) is the dominant consumer of energy from the battery, typically consuming as much energy as the sum of all other components in the transceiver. Much of the energy consumed is dissipated as heat due to the relative inefficiency of the PA. Traditionally the market for mobile PAs has been dominated by III-V Semiconductor compounds due to higher peak efficiency and larger output power (due to better breakdown characteristics). Recent research on CMOS switching PAs in combination with linearization techniques such as envelope elimination and restoration (EER), out-phasing and pulse width modulation (PWM), have shown the possibility for better average efficiency than a linear PA using III-V devices. In addition to the ability to improve the average efficiency of the PA, the ability to integrate the PA allows for true system-on-a-chip radios and potential cost savings compared to current wireless architectures. Current EER solutions need significant digital calibration or use of feedback to correct for delay mismatches between the envelope and phase signal paths. We propose to incorporate the envelope and phase signals into the same path in order to minimize the delay mismatch between the signals and mitigate the need for calibration.

Design Automation Techniques for Minimizing Dynamic and Static Energy Consumption in Multicore and Mixed-Signal, Wireless Sensor Systems

Patrick Yin Chiang (Oregon State University)

Abstract - Power consumption and energy efficiency are critical requirements for future microelectronics. These considerations are essential for both ends of the processor spectrum – from high-end, multicore computing that is used in cloud-computing servers, to energy-scavenging, sub-threshold operation, wireless sensor SoCs. While there has been an enormous amount of recent work in this ultra-low power arena (sub/near-threshold digital logic presented by D. Blaauw, A. Chandrakasan, K. Roy), design automation and the ability to automate these new sub/near-threshold methodologies into standard mixed-signal flows with minimal design time, reliability, and testability is still severely lacking. We propose in this work design automation techniques for implementing low-voltage swing interconnect and sub/near-threshold digital design in both multicore and ultra-low power, mixed-signal applications. The two components focused in this project are: A) energy-efficient on-chip interconnects, including design automation of low-voltage swing interconnects into standard synthesis flow; B) design techniques for compensating for excessive delay variations of synthesized logic, including standard cell culling and Razor-like, near-threshold delay detection circuits.

Low-Power Low-Jitter All-Digital Frequency Synthesizers

Pavan Kumar Hanumolu (Oregon State University)

Abstract - The goal of our proposed research is to explore and invent system and circuit-level design techniques that will enable ultra low-power clock generators. Particular emphasis is on the implementation of digital frequency synthesizers that have excellent jitter performance over a wide operating range and have excellent immunity to supply noise at all frequencies. To this end, we propose: (a) three digital supply noise cancellation schemes, (b) intrinsic oscillator phase noise suppression

techniques, and (c) low-jitter, all-digital clock generators employing the proposed techniques. With the aid of the proposed techniques, we seek to achieve lower than 2 percent, long-term r.m.s jitter with better than 0.25mW/GHz power efficiency.

Low Noise Highly Linear Wideband MMICs for Multi-band Beamformer Applications

Deuk Heo (Washington State University)

Abstract - The existing beamforming systems on silicon are mostly narrow band and span only a few bands of interest. Conventional techniques that are applied to improve bandwidth, noise figure and linearity are not sufficient to meet performance requirements for multi-band operations in the low voltage scaled silicon process. We propose to advance the current state-of-the-art Rx beamforming chipset by optimizing the performance of each key sub-block in terms of linearity, noise, bandwidth, and phase accuracy. The research objective is to investigate high-performance MMICs for ultra wideband, highly linear beamformer chipsets for phased array communication systems from Ku to Ka bands, which cover the operating frequency ranges of satellite communications and terrestrial microwave communications. For high performance and low-cost phased array systems, we propose a highly integratable single-channel Rx chipset, which is easily scalable to multi-channel multi-beam Rx beamformers. Based on scaled silicon-based technologies, key sub-blocks including wideband low noise amplifiers, wideband variable gain amplifiers with reduced phase error, and highly linear active phase shifters will be investigated and implemented. For all these sub-blocks, novel design methods are utilized to extend bandwidth and enhance linearity.

High-Throughput Data Busses

George La Rue (Washington State University)

Abstract - As CMOS technology continues to scale with higher speed, density and integration levels, input/output (I/O) capacity becomes even more of a bottleneck. Many member companies have applications where large amounts of data need to be communicated among chips, boards and/or systems. We are investigating transceiver design in the 80 Gbps to 100 Gbps range in 65 nm CMOS technology. Simulations using extra-delayed-clock (EDC) flip-flops without inductors show operation above 100 Gbps in a half-rate clocked multiplexer. To achieve enough bandwidth for operation at these high rates the Common Mode Logic (CML) clock buffers require inductors that tend to dominate layout area. We have made good progress to reduce layout area of these inductors to lower manufacturing cost of high-speed transceivers. Fabrication of a serial link test chip including a transmitter with pre-emphasis, a receiver with analog equalizer and inductor and amplifier test structures will begin this summer. After fabrication, we will use the test chip to investigate packaging and printed circuit board (PCB) requirements for operating at these high rates. In addition, we will also design clock and data recovery (CDR) circuits and PLL synthesizers needed to form fully-integrated serial links. We will include test structures for PLLs using both LC VCOs for lower jitter and ring VCOs for wider tuning ranges. We will then design and layout a second serial link test chip that will include these synthesizers, a CDR along with improvements to the transmitter and receiver designs based on knowledge gained from testing the first chip. Our second design will make use of improved inductor and transformer models based on results of the test structure measurements from the first fab. In addition, we will complete testing of the single-ended data bus test chips that we expect to receive in June.

Power Efficient Analog Circuits in CMOS

Un-Ku Moon (Oregon State University)

Abstract - The recent popularity of mobile systems makes power consumption of the system one of the key performance parameters in various applications. Furthermore, the recent trend with system-on-chip (SoC) is to largely merge several functions into a single chip and in line with technology scaling. Since by definition SoC integrates a large number of analog blocks, the power efficiency of those analog blocks as well as digital circuits that service those analog blocks become very important in the SoC circuit design paradigm. Among the various analog blocks embedded into modern systems, analog-to-digital converters (ADC) play an important role and are key to the targeted overall system performance. Especially in advanced wired and wireless communication systems, which attempt to achieve higher performances, the demand for high resolution and wide signal bandwidth with low power consumption in their associated ADCs is further increased. The thrust of this project is to develop new ADC architectures and circuit techniques which enable high performance in terms of the resolution and bandwidth, while at the same time reducing power consumption. We will pursue these goals in the context of submicron CMOS scaling.

Ultra Low-Power Adaptive Radio Receiver Architectures and Circuits for Wireless Sensing

Brian Otis (University of Washington)

Abstract - For complete energy autonomy of the wireless sensing networks running on harvested energy, their power dissipation must be on the order of $100\mu\text{W}$. Both the peak and average power dissipation of the node must be minimized since small batteries and energy harvesters exhibit regrettably large source impedances. The radio transceiver typically consumes the bulk of the total power; its own peak/average power consumption must fall below $100\mu\text{W}$. In the past year, we successfully tackled the problem of realizing a highly-integrated sub- $100\mu\text{W}$ 400MHz CMOS transmitter with the highest reported global efficiency and the lowest overall power dissipation to date. In this project, we will investigate new adaptive receiver architectures and circuit techniques that will permit 400MHz sub- $100\mu\text{W}$ operation without sacrificing performance. We predict that the proposed work will result in a $4\times$ improvement in the state-of-the-art. The new architecture and techniques can easily be extended to higher frequency bands as well.

Micro-Power Data Converters

Jacques Chris Rudell (University of Washington)

Abstract - Overall current consumption of mobile transceivers for commercial applications is often dominated by the Power Amplifier (PA) power efficiency. This is particularly true for 4th Generation (4G) standards which use different flavors of OFDM signal modulation which inherently requires high-linearity of the transmit signal path, to accommodate high signal Peak-to-Average Ratios (PAR). Although many aspects of PA design influence performance such as the circuit topology and the technology used for implementation, the output load presented to the PA will heavily impact Power Added Efficiency (PAE) and linearity. Traditional PA design methods often seek an optimal load impedance, R_{opt} , by performing a load pull simulation or measurement. The antenna impedance is then transformed to R_{opt} at the PA output by way of a matching network. However, the PA output impedance required for optimal performance may change as a function of variations in PVT or by a fluctuation in antenna impedance. This project seeks to explore new methods to calibrate and optimize the PA output load impedance using a fully integrated system. The research conducted by the PI over the next

year will explore methods of tuning integrated baluns, transformers and power combining structures to deliver the optimal real part load impedance. The proposed research will be, to the PIs best knowledge, the first integrated tuning method for on-chip transformers and power combining structures. This project will further explore methods towards phase tuning between primary paths in a power combining structure.

Micro-Power Data Converters

Gabor Temes (Oregon State University)

Abstract – The purpose of the proposed research is to develop micro-power data converters, both ADCs and DACs. Micro-power A/D converters are often needed in sensor networks used for environmental monitoring, medical sensors and probes, industrial control, security and other applications where power is provided by batteries or energy scavenging, and hence it is very limited. Micro-power DACs may be used in micro-stimulators and micro-actuators in biomedical applications. Under the proposed research, we shall continue the development of novel and efficient micro-power data converters, both analog-to-digital and digital-to-analog ones, which can be used in the most common biomedical and environmental applications.

Enabling Metal-Fill-Aware Design of RF/Mixed-Signal Integrated Circuits

Andreas Weisshaar (Oregon State University)

Abstract - The objective of this project is to enable metal-fill-aware design of RF/analog and mixed-signal integrated circuits. The approach is to make metal fill cells an inherent part of the design and layout process and develop design guidelines for the placement, shape and size of metal fill cells near interconnects and passive components. The main passive structures for this investigation are single and coupled microstrips, MIM capacitors, and spiral inductors. For this period the benefit of our effective-dielectric-constant-based capacitance formulation is applied to on-chip microstrips and spiral inductors. The formula reduces memory requirements and provides more than doubling of simulation speed. Application of the formula for microstrips matches simulations and measurements. For a spiral inductor a 3,000-fold increase in speed is observed. We have developed a closed-form empirical expression appropriate for calculating eddy currents in a uniform magnetic field accurate to within 6%. We present simulation-based metal fill size and shape recommendations for single and coupled microstrip transmission lines. We have fabricated a chip in the Jazz CA18HX 0.18 μ m RF CMOS process to validate our conclusions, and preliminary measurements confirm the metal fill design trends for eddy-current loss and capacitance increase due to fills. Our technique to reduce the substrate capacitance of MIM capacitors is successfully tested in a 0.25 μ m BiCMOS process. In this project, we plan to further develop our metal fill analysis formulas and begin applying the techniques to enable scalable modeling. The empirical eddy-current expression will be extended to non-uniform and off-angle fields. We then plan to implement a scalable EM modeling tool to analyze square and octagonal spiral inductors. To aid in circuit simulation, a lumped-element equivalent circuit Spice/Spectre model will be extracted from the scalable model's frequency-dependent S-parameters. Finally we hope to develop a CAD tool incorporating the scalable modeling algorithm. We plan to test our tool's accuracy with fabricated test structures.