

# CDADIC RESEARCH TOPICS FY09

## - IAB VOTES -

CIRCUIT DESIGN	VOTES
On-die thermal sensors	2
Low jitter PLLs without inductors	2
NBTI insensitive analog circuits (NBTI: negative bias temperature instability)	
Combination DLL/PLL clock distribution schemes	1
Wide range/high accuracy temp. sensor with single temp trim point (must maintain +-1% accuracy from 0-120	
Si/SiGe PAs	2
Analog designs at cryo-temperatures	
RF switches – MEMs and silicon only solutions	5
SiGe Design for WCDMA Front End	
High-Speed, High SFDR DACs in <0.18µm Digital CMOS 90dB, 100MHz	1
Improved CMOS Bandgap Reference (<1% Absolute, <20ppm)	1
Bi-CMOS Optimized Mixed-Signal Designs	
High-Speed (>10msps 14+ bits) ADC+DACs	5
Low-Phase Noise Submicron VCOs	4
High-Voltage Op Amps in Low-Voltage CMOS Processes	1
Low-Power, Low-Drift Precision References on Standard CMOS Processes	2
Continuous-Time Delta-Sigma Multi-Bit ADC/DACs	2
Low-Cost 5.6 GHz RF Circuits & Down Conversion Receivers	
Micro-Power Biasing Techniques (on-chip sub 1uA, constant gm, etc.)	1
Adaptive Digital Error Cancellation in Data Converters	2
High-Performance Sample-and-Holds	
Substrate Noise Coupling Models for Mixed-Signal Design	1
Micro-Power Data Converters (16+bits, 100uW, etc.)	3
Adaptive DSP Compensation for Analog Distortions in 2.4 & 5.8 GHz Transceivers	1
Precision ASIC Cells for Wide Temperature	
Phased-Array Antenna Circuit Elements	1
Switched-Capacitor Circuits in Digital CMOS Technology	1
SiGe Data Acquisition Circuits up to 30GHz	1
RF Power Amps	4
RAD Hard CMOS Mixed-Signal Circuits Design	
GaAs/InP ADC (250 MHz, 14-16 bits; 1gsps @ 12 effective bits)	
High-Sensitivity Low-Noise CMOS Imagers	
CMOS Imager Architectures for Very-High Resolution Arrays	
Ultra-High Speed Digital Circuit Synthesis & Layout	1
Multiple Input – Multiple Output DC/DC Converters	1
Driving-Switched Cap Loads Quickly & Accurately at Low Power	
High Dynamic Range Filters as in those used in IF Stages	1
Mixers with High Image Rejection (>30dB)	1
High IP3, Low-Voltage Supply CMOS Elements; Amps, Mixers, etc.	3
Ultra-Low Power Standard Analog Elements Designs	3
Ultra-Wideband 2-10.5 GHz Circuits	1
Reconfigurable Systems for Flexibility or for Self-Healing	2
Digital Beam Forming Methods for Phased-Array Antennas	1
Very High Speed Serializer - Deserializer	2
Sub 1Volt Supply Bandgap Reference	1
Capacitive Sensor Circuits	2
Substrate Noise Immune Circuit Topologies	
Low Cost SiGe 11 - 15GHz LNA, PA, Switches, Attenuators	1
Ultra-Low Power Radio	2
1/f Noise Immune VCOs	1
Ultra Low Power Digital Circuits	
Acoustic Charge Transport Devices or CCDs for Tunable HF High Q Filters	
Leakage Immune Analog Design	2
Multiple Voltage Range Analog on Low V CMOS	2

Low Phase Noise Logic Techniques	2
High Temp (200C) Analog Designs	
Clockless Logic in Mixed Signal Communications	
Novel Non-Volatile Memory for Rad Hard & Embedded Designs	
Very High Dynamic Range Low Cost Circuits	
Equalizers for 5GHz+ and Adaptive Equalization for Line Drivers	2
Circuit Design for Automatic Crosstalk Noise Cancellation	
High Impedance Current Source GaAs/InP	
<b>MODELING AND SIMULATION</b>	
Single Event Effects Modeling and Mitigation Methods Including Automated Analysis Tools	1
Modeling of Long Term Device Drift Including Package Effects	
Integrated Thermal and Electrical Modeling Simulation	
Integration of Substrate Noise Models with Industry Tools (practical implementation)	
ESD Modeling for CMOS Plus Simulation Models	1
On-Chip Interconnect Models for High-Frequency/Speed Integrated Circuits on Silicon Substrate	
Deep-Submicron Analog Layout Automation for Performance & Manufacturability	3
Simulation of Noise in Nonlinear Circuits	
Behavior Modeling of RF Circuit Blocks & Development of RF Circuit Models	1
Analog CAD – Synthesis Methods	2
Universal Models for Device Stress & Failure Analysis	
CMOS RF Power Transistors and Amplifiers Modeling & Simulation	
Efficient Thermal Behavior of Packaged Integrated Circuit Devices	
Efficient Mix-Mode Schematic Capture, Simulation and Layout	
Sealable Modeling and Design of Embedded Passives	1
Analog Accurate and Characterizable MOS Models for Deep Sub-Micron with Open Access Hooks	
Single Event Modeling and Mitigation Methods for Deep Sub-Micron	
SiGe, and Trench SiGe Substrate Noise Coupling Over Frequency	1
Radiation Effects on 1/f Noise Both Modeling and Characterization	
SOS Modeling	
High Frequency Package Effects Modeling	1
MOS Noise Modeling in Different Operating Regions, HF Noise Modeling	
Accurate Models of Single Event Transients and Effects	
Automated Single Event Analysis Tools	
Tools for Predictive Design in Very Deep Submicron Circuits (less than 100 nm)	
Automatic Speed Power Optimization of Mixed Signal & RF Designs	1
Cost, area & power effectiveness of moving analog to nanoscale technologies	3
<b>TEST</b>	
Test and Evaluation/Verification	1
Built in Analog and RF Self Testing	2
Scaleable and Transportable Reliability Coupons	
Fast Converging PLL	